SEMICONDUCTOR SWITCHING DEVICE WITH FUNCTION FOR VIBRATING CURRENT, THEREBY SHUTTING DOWN OVER-CURRENT

CROSS REFERENCE TO RELATED APPLICATIONS

The subject application claims benefit of the earlier filing dates of Japanese Patent Application Nos.2000-222982 and 2000-363644 filed on July 24, 2000 and November 29, 2000 under the Paris Convention, the entire contents of which are incorporated by reference herein.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor switching device for detecting and shutting down an over-current due to current vibration. More particularly, the present invention relates to a semiconductor switching device capable of detecting an over-current even when a rush current flows a load such as a lamp load or a motor load.

2. Description of the Related Art

A conventional semiconductor switching device (power semiconductor device) is employed for power supply control. The conductor switching device selectively supplies a battery power to respective loads in automobile. The semiconductor switching device controls power supply to a load by an incorporated thermal FET.

The semiconductor switching device has a shunt resistor. One end of the shunt resistor is connected to a power VB for supplying an output voltage VB, and further a drain terminal of the thermal FET is connected to the other end. Further, a load is connected to a source terminal of the thermal FET. This load is directed to an automobile headlight or power window driving motor and the like. The semiconductor switching device is provided with an A/D converter and a microcomputer (CPU) for controlling a drive signal of the thermal FET to be turned ON/OFF based on a current value monitored by this shunt resistor. Further, this semiconductor switching device has a driver for controlling the thermal FET to be driven based under the control of the A/D converter and microcomputer (CPU).

The thermal FET incorporates a power device (mainly FET), a resistor, a temperature sensor, a latch circuit, and an overheat shutdown FET. These elements configure a gate shutdown circuit. A gate shutdown circuit

comprises an overheat shutdown function for controlling the thermal FET (power device) to be forcibly turned OFF in the case where a junction temperature of the thermal FET rises up to a predetermined temperature or higher. In the case where it is detected by a temperature sensor that the power device (mainly FET) rises at a predetermined temperature or higher, the detection information is maintained in the latch circuit, the overheat shutdown FET of a gate shutdown circuit is operated to be turned ON, and the power device is controlled to be forcibly turned OFF.

However, a shunt resistor is connected in series to a power supply path in order to detect a current. There is a problem that a thermal loss of the shunt resistor due to a large amount of load current in recent years cannot be ignored.

In addition, the above described overheat shutdown function and the gate shutdown circuit functions in the case where a substantially complete short-circuit state is generated with a load and a wire, and a large amount of current flows. However, the overheat shutdown function does not function in the case where a small amount of short-circuit current such as so called rare short flows, which includes an incomplete circuit having a certain degree of short-circuit resistance.

A current is monitored, and an over-current is detected by means of a microcomputer, whereby the thermal FET can be controlled to be turned OFF. However, there has been a problem that response properties caused by microcomputer control is impaired respect to such over-current.

In addition, a shunt resistor, A/D converter, and a microcomputer and the like are required, thus, a large packaging space is required. Moreover, there is a problem that the equipment cost is increased by these comparatively expensive elements.

Further, in the case where a lamp load is used as a load, when a voltage is applied to the lamp load, there flows a rush current that is about 10 times as large as when the lamp load is used. Conventionally, when a current is detected without being limited to the above method, this rush current is masked, and is not detected. In the case where the lamp load or the like are used, the rush current is masked, and is not detected. Thus, the detection of over-current is delayed, and the switching device or wire has been excessively heated.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a semiconductor switching device capable of detecting an over-current even when a rush current flows, the semiconductor switching device having a thermal loss and shutting down an over-current such as incomplete short-current at a high speed.

In order to achieve the foregoing problems, according to a feature of the present invention, there is provided a semiconductor switching device comprising:

a multi-source FET that including a main electric field effect transistor (FET) and a reference FET;

a reference current setting circuit for feeding a reference current including a constant component current and a transient component current to the reference FET such that a source potential of the main FET is not lower than that of the reference FET when a load current flowing a main FET is not within the range of an over-current containing a transient component;

a voltage comparator for detecting that the source potential of the main FET is lower than that of the reference FET;

a counter for counting the number of times of variation of the reference voltage vibration number of times to a predetermined number of times; and

a gate driving circuit for turning OFF the main FET by counting the counter. This makes it possible to shut down a current without the presence or absence of a transient component if a current exceeding a normal range flows a current on the load side.

Other and further objects and features of the present invention will become obvious upon an understanding of the illustrative embodiments about to be described in connection with the accompanying drawings or will be indicated in the appended claims, and various advantages not referred to herein will occur to one skilled in the art upon employing of the invention in practice.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

Fig. 1 is a block diagram showing a semiconductor switching device with a current vibration type shutdown function according to the present invention;

Fig. 2 is a circuit configuration diagram showing a first semiconductor switching device with a current vibration type shutdown function;

Figs. 3 to 6 are signal waveform chart of a first semiconductor switching device with a current vibration type shutdown function in a first embodiment of the present invention (the normal use of a load), where Fig. 3 shows the waveforms of VSA, n x Iref, and ID respect to a 200 ms timer signal, Fig. 4 shows the waveforms of VSA, n x Iref, and ID respect to a 20 ms timer signal, Fig. 5 shows the waveforms of VSA, n x Iref, and ID when a switch SW1 is turned ON, and Fig. 6 shows a time axis that is 10 times as large as when compared with Fig. 5;

Figs. 7 and 10 are signal waveform charts of a first switching device with a current type shutdown function in a second embodiment of the present invention (in the case where a overload state is made transition during the normal use of a load), where Fig. 8 shows in the case where the switch SW1 of Fig. 7 is turned ON by enlarging a time axis to 2,000 times as compared with Fig. 7, Fig. 9 shows in the case where the shutdown function of Fig. 7 works by enlarging a time axis to 400 times as compared with Fig. 7, and Fig. 10 shows in the case where the shutdown function of Fig. 9 works respect to the waveforms of a voltage at point A (dummy voltage) and VSA by further enlarging a time axis to 5 times as compared with Fig. 9;

Fig. 11 is a signal waveform chart of a first semiconductor switching device with a current vibration type shutdown function in a third embodiment of the present invention (in the case where an overload state is established after use of a load has been started);

Fig. 12 is a circuit configuration diagram showing a second semiconductor switching device with a current vibration type shutdown function according to the present invention;

Fig. 13 is a view for illustrating FET shutdown by using a continuous 4-pulse counting system of a second semiconductor switching device with a current vibration type shutdown function;

Figs. 14 to 17 are signal waveform charts of a second semiconductor switching device with a current vibration type shutdown function in a fourth embodiment (normal use of a load), where Fig. 14 shows the waveforms of VSA, n x Iref, and ID respect to a 20 ms timer signal, Fig. 15 shows the waveforms of VSA, n x Iref, and ID when a switch SW1 is turned ON, Fig. 16 shows that a time axis is displayed to be enlarged to 10 times as compared

with Fig. 15, and Fig. 17 shows the waveforms of VSA, n x Iref and ID respect to a 200 ms timer signal;

Fig. 18 is a signal waveform chart of a second semiconductor switching device with a current vibration type shutdown function in a fifth embodiment of the present invention (in the case where a dead short state is established after use of a load has been started;

Fig. 19 is a signal waveform chart of a second semiconductor switching device with a current vibration type shutdown function in a modified example of the fifth embodiment of the present invention (in the case where a dead short state is made transition during the nomal use of a load);

Fig. 20 is a signal waveform chart of a second semiconductor switching device with a current vibration type shutdown function in a sixth embodiment of the present invention (in the case where an overload state is made transition during the nomal use of a load);

Figs. 21 to 23 are signal waveform charts of a second semiconductor switching device with a current vibration type shutdown function in a seventh embodiment of the present invention (in the case where an overload state is made transition during the nomal use of a load), where Fig. 22 shows in the case where the switch SW of Fig. 21 is turned ON by enlarging a time axis to 5,000 times as compared with Fig. 21, and Fig. 23 shows in the case where the shutdown function of Fig. 21 works by enlarging a time axis to 5,000 times as compared with Fig. 21;

Fig. 24 is a flow chart of a current vibration type shutdown function of a semiconductor switching device 1 according to the present invention;

Fig. 25 is a flow chart of the steps at which a reference current vibrates; and

Fig. 26 is a flow chart of the steps of feeding a reference current.

DETAILED DESCRIPTION OF THE EMBODIMENTS

Various embodiments of the present invention will be described with reference to the accompanying drawings. It is to be noted that the same or similar reference numerals are applied to the same or similar parts and elements throughout the drawings, and the description of the same or similar parts and elements will be omitted or simplified.

Fig. 1 is a block diagram showing a semiconductor switching device 1

with a current vibration shutdown function according to the present invention.

A semiconductor switching device 1 has a multi-source FET (Tr5) including a main electric field effect transistor (FET) (QA) and a reference FET (QB).

This device 1 has a reference current setting circuit 11. This circuit 11 feeds a reference current Iref including a constant component current Irefc and a transident component current Iref to the reference FET (QB) such that a source potential VSA of a main FET (QA) is not lower than a source potential VSB of the reference FET (QB) when a load current ID flowing this main FET (QA) is not within the range of an over-current including the transient component.

The device 1 has a voltage comparator CMP1 for detecting that VSA is lower than VSB.

The device 1 has counters (4, 14) for counting the vibration number of times of the reference current (Iref) to a predetermined number of times by detecting that this voltage comparator (CMP1) is low.

The device 1 has a gate driving circuit (8) for turning OFF the main FET (QA) by counting this counter. This makes it possible to shutdown a current irrespective of whether a transient component is present or absent when a current exceeding a normal range flows a current ID on a load side.

Moreover, in the device 1, as long as a load current is within the normal range, the voltage comparator (CMP1) detects that VSA is not lower than VSB, whereby the gate driving circuit (8) turns ON the main FET (QA) and the reference FET (QB).

In the device 1, a reference current (Iref) vibration method includes some patterns. First, the feeding of a transient component current (Ireft) is repeatedly started, whereby the reference current (Iref) vibrates.

Moreover, this starting time intervals are a third predetermined time or less.

In the case where only the constant component circuit 14 operates or in the case where the constant component circuit 14 and transient component circuit 13 operate, when the source potential VSA of the main FET (QA) is lower than the source potential VSB of the reference FET (QB), if a phenomenon that a transient component circuit 13 is restarted, and the transient component circuit 13 is further restarted again within a third

predetermined time after the restart is repeated predetermined number of times, the main FET (QA) is shut down. The third predetermined time is set as a time capable of detecting a next generated over-current which starts when and after the last over-current has been detected while the over-current detection number of times is counted. That is, if an over-current is detected within a third predetermined time, the number of times is integrated; and however, If an over-current is not detected after the third predetermined time has elapsed, the detection number of times is cancelled. This is because only a continuously generated over-current is targeted for detection. If the starting of the transient component is disabled within the third predetermined time without this cancellation, A problem occurs when this device is used as a fuse on the upstream side of a plurality of load. That is, when a first load is turned ON, whereby the transient component starts, and then, when the transient component current decreases, if a second load starts within the third predetermined time, a transient component Ireft of a reference is reduced. Thus, there is a possibility that the source potential VSA of the main FET is lower than the source potential VSB of the reference FET. In addition, the starting of the reference transient component Ireft is restricted. Thus, the main FET (QA) is shut down at that time. A problem occurs when two loads are turned ON with a time different equal to or less than the third predetermined time, and therefore, this shutdown is effective as a solution to the above problem.

The transient component current Ireft may be a constant current, and may be a current whose waveform is analogous to the transient component of a load current ID. After an elapse of a fourth predetermined time, the transient component current Ireft of the reference FET is eliminated, and only the constant component Irefc is present. At this time, the transient component current may flow the load 10 side. At this time, the transient component Ireft of the reference restarts, and thus, the FET (QA) is never shut down. In the case where the fourth predetermined time is shorter than a transient component continuation time at the load 10 side, a reference transient component circuit 13 starts a plurality of times. As long as the start count of the transient component Ireft for FET (QA) shutdown is set to be greater than this time, the FET (QA) is never shut down due to a transient current component of a normal load. A protection function for shutting down the FET (QA) can be achieved only if an over-current occurs.

In addition, in the device 1, a reference current Iref vibration method includes the following patterns. The main FET (QA) and the reference FET (QB) repeat ON/OFF operations, whereby the reference current Iref vibrates. The counters 4, 14 count the vibration number of times within the second predetermined time or less. In the case where a predetermined number of times is not counted within the second predetermined time, it can be assumed that the load current ID has been released from an over-current state.

Moreover, ON/OFF operation is repeated as follows.

First, the voltage comparator CMP1 detects that the source potential VSA of the main FET is lower than the source potential VSB of the reference FET, whereby the gate driving circuit 8 turns OFF the main FET (QA) and reference FET (QB).

A dummy voltage setting circuit 2 sets a first potential (potential at point A) that is lower than VSA.

The voltage comparator CMP1 detects that the lowering VSM is lower than the first potential, whereby the gate driving circuit 8 turns ON QA and QB.

The dummy voltage setting circuit 2 sets a second potential (potential at point B) that is greater than the first potential (potential at point A).

The voltage comparator CMP1 detects that the increasing VSB is greater than the second potential and is greater than VSA, whereby the gate driving circuit 8 turns OFF QA and QB.

From these facts, as long as VSA is lower than VSB, ON/OFF operation can be continued.

A reference current setting circuit 11 comprises a constant component circuit 14 for feeding a constant component current Irefc and a transient component circuit 13 for feeding a transient component current Ireft. In the case where VSA is equal to VSB, a voltage obtained by dividing a load current ID that flows QA by a reference current Iref is defined as "n". A constant component current Irefc is greater than a value obtained by dividing by "n", a current value in a constant state when the load current ID is not within the range of an over-current. The transient component current Ireft is greater than a value obtained by dividing by "n", a current value of a transient component in a transient state when the load current ID is not within the range of an over-current. Therefore, a current indicating an upper limit (within a normal range) which is not within the range of an over-current can

be fed to QB transiently.

In addition, the constant component circuit 14 can be composed of a resistor R6 or a constant current circuit. The constant component circuit 14 can be formed by using the resistor R6. In addition, a constant current Irefc can be fed constantly by using the constant current circuit.

The constant component current 14 feeds the constant component current Irefc when the load current IF flows. Thus, when QA is turned ON, QB is set to an ON state, making it possible to detect a current.

The transient component current Ireft is first fed within a first predetermined time and at a constant current value. Next, within a second predetermined time after the elapse of the first predetermined time, the above current is decreased within a range such that VSB does not exceed VSA, and is set to almost zero. This decrease is achieved by a time constant determined by electric discharge characteristics in which the charge accumulated in a capacitor C1 is discharged via a resistor R8. Thus, current indicating an upper limit within the normal range can be supplied constantly while its deviation is reduced.

The voltage comparator CMP1 detects that VSA is lower than VSB, whereby the transient component circuit 13 starts feeding the transient component current Ireft. However, restarting is not effect within the second predetermined time. Thus, the second predetermined time can be acquired as a time from over-current detection to judgment of whether or not a current is finally shut down.

A predetermined count in the first predetermined time is less than that in the second predetermined time. This makes it possible to detect an over-current in two patterns within the predetermined first and second time. Within the first predetermined time, a large over-current can be detected within a short time. With the second predetermined time, the over-current is detected for a long time, thus making it possible to precisely detect a small over-current.

This semiconductor switching device 1 operates while the device is connected between a power source VB for supplying an output voltage VB and a load 10. In addition, the device 1 is connected to the resistor 6 and capacitor C1. The resistor 6 and capacitor C1 are connected to each other, whereby the device 1 has the functions described below. The resistor 6 and capacitor C1 are provided externally of the device 1 such that a resistance

value and a capacity value can be changed according to the load 10. A switch SW1 is also led externally of the device 1 so as to enable remote operation of the device 1. The switch SW1 is connected, whereby the device 1 has the functions described below. A region indicated by dotted line of the device 1 shown in Fig. 1 indicates a region in which integration can be effected.

However, the device 1 uses a multi-source electric field effect transistor (FET) Tr5 as a main device (power device) in the circuit 1. Although the multi-source FET (Tr5) allocates an overheat shutdown circuit 9 in the vicinity of the FET, this overheat shutdown current 9 is not essential in the case where a constant current is fed, as is understandable from a description given later. The multi-source FET (Tr5) comprises a main FET (QA) and a reference FET (QB), wherein gate electrodes of QA and QB are connected to each other, and their drain electrodes are connected to a power source VB. The QA source electrode is connected to a "+" input terminal of the comparator CMP1, and the QB source electrode is connected to a "-" input terminal of the comparator CMP1.

As this multi-source FET (Tr5), for example, there can be used a power MOSFET with a DMOS structure, a VMOS strucure, or a UMOS structure, a MOSSIT with a structure analogous to these structures instead of the FET. In addition, a MOS composite type device such as EST and MCT, or another insulation gate type power device such as IGBT can be used. Further, if a gate is used as a reverse bias, a junction type FET, a junction type SIT, SI thyrister and the like can be used. This Tr5 may be "n" channel type or "p" channel type.

The semiconductor switching device 1 comprises: at least a multi-source FET (Tr5); a comparator means (CMP1) for comparing voltages of the QA and QB source electrodes with each other; and a driver 8 for supplying a control voltage to a gate electrode of Tr5 according to an output of this comparator means (CMP1).

As this QA, for example, there may be employed a power device with a multiple channel structure in which a plurality of unit cells are connected in parallel. QB is allocated at a position adjacent to QA so as to be connected in parallel to the QA. QB is allocated at a position adjacent to QA in the same process, such that a deviation in electrical characteristics caused by an effect of non-uniformity between a temperature drift and a lot can be eliminated. The number of unit cells connected in parallel, each of which configures QB,

is adjusted such that the QB current capacity is smaller than the QA current capacity. For example, the number of QA unit cells is configured to be 1,000 respect to one QB unit cell, whereby a ratio in channel width W between QB and QA is defined as 1:1,000. This ratio is equal to a ratio between a current flowing QB and a current flowing QA in the case where the QA source potential is equal to the QB source potential. In this way, the current flowing QB can be reduced.

In addition, a diode connected to the overheat shutdown circuit 9 functions as a temperature sensor. This diode is formed by a polysilicon thin-film deposited at the upper part of an inter-layered insulation film formed at the upper part of QB and QA, and a plurality of diodes are connected in series. As a temperature of QA rises, an overheat is detected by a voltage fall at both ends of a plurality of diodes connected in series.

More specifically, the semiconductor switching device 1 with its current vibration type shutdown function comprising: a dummy voltage setting circuit 2 for controlling the voltage of "+" input terminal (dummy voltage) of CMP 1; a pulse counter 4 for counting the number of times from H to L of an output signal of CMP1; a timer 3 for specifying a count time of the counter 4; a shutdown signal holding circuit 5 for holding a shutdown signal output after a predetermined number of times has been counted by the counter 4; a chattering prevention circuit 6 for preventing a chattering of an external input signal that is an ON signal of the switch SW1; a source transistor having a collector side connected to a potential VP; and a sink transistor having an emitter side connected to a grounding potential (GND), these elements being connected in series, as well as Tr5, comparator CMP1, and overheat shutdown circuit 9. The semiconductor switching device 1 further comprising: a driver 8 for controlling a source transistor and a sink transistor to be turned ON/OFF based on a switch signal or the like caused by turning ON/OFF switch SW1, and outputting a control signal to a gate electrode of Tr5; a charge pump 7 for increasing a pressure to a potential VP; a reference current (Iref) setting circuit 11 for generating a transient current component of a reference current Iref for judging whether or not a rush current generated at a lamp load is an over-current. The switching device 1 is mounted in a monothilic manner on the same semiconductor substrate (semiconductor chip). The resistor R6 and capacitor C1 are provided externally of the chip. By externally providing these elements, the

respective resistance value and capacity value can be easily changed, and the waveform of a reference current can be traced respect to the waveform of such rush current.

Next, a current vibration type shutdown function of the semiconductor device 1 according to the present invention will be described with reference to the flow charts shown in Figs. 24 to 26. This device 1 vibrates a current, thereby detecting an over-current and shutting down the over-current. Hereinafter, a method of detecting and shutting down the over-current will be described.

First, in order to perform switching that is a basic function of the device 1, as shown in the step S1 of Fig. 24, a driver 8 turns ON a main FET (QA). A load current ID flows. Next, as shown in the step S2, in a reference current circuit 11, a reference current Iref including a constant component current Irefc and a transient component current Ireft is fed to QB such that the QA source potential VSA when the ID flowing QA is not within the range of an over-current including a transient component is not lower than the source potential VSB of the reference FET (QB).

At the step S3, the voltage comparator (CMP1) detects generation of an over-current based on the fact that VSA is lower than VSB. On the other hand, it is assumed that an over-current is not generated. Then, processing reverts to the step S1.

In the case where an over-current is generated, the timer 3 is started in the step S4.

At the step S5, the reference current Iref vibrates. During vibration, an over-current is generated.

At the step S6, the counter 4 counts the vibration count of the step S5. Thus, a time when an over-current is generated is indirectly measured.

At the step S7, the counter 4 judges whether or not the vibration number of times reaches a predetermined number of times. If it reaches the predetermined number of times, it is assumed that an over-current flows continuously for a predetermined time or more. That is, it is judged that this over-current is not temporary. At the step S8, the driver 8 turns OFF QA.

If it does not reach the predetermined number of times, it is judged whether or not the timer 3 reaches a predetermined time in the step S9. If it does not reach the predetermined number of times, processing reverts to the step S5 and vibration and the number of times are counted. If it reaches the

predetermined number of times, it is judged that the detected over-current is temporary. At this time, QA is not shut down. Then, processing reverts to the step S1 and a next over-current detection is ready.

Moreover, the vibration in the step S5 may be directed to repeatedly starting feeding of the transient component current Ireft. The starting time intervals are equal to or less than a third predetermined time. Based on this fact, it may be judged that an over-current continues.

In addition, the vibration in the step S5 may be directed to QA and QB repeating ON/OFF operation.

This QA and QB repeating of ON/OFF operation is effected according to the flow chart shown in Fig. 25.

First, same as the step S3 shown in Fig. 24, in the step S11, the voltage comparator (CMP1) detects generation of an over-current by the fact that VSA is lower than VSB. Otherwise, it is assumed that an over-current is not generated. Then, this repeating of ON/OFF operation is stopped.

By detecting generation of an over-current, the driver 8 turns OFF QA and QB in the step S12.

At the step S13, the dummy voltage setting circuit 2 sets a first (point A) voltage that is lower than VSA.

At the step S14, the CMP1 detects that falling VSB is lower than the first potential (potential at point A).

At the step S15, the driver 8 turns ON QA and QB.

At the step S16, the dummy voltage setting circuit 2 sets a second potential (potential at point B) at which the rising VSB is greater than the first (point A) potential.

At the step S17, it is detected that VSB is greater than a second potential (potential at point B). Then, processing reverts to the step S11.

Next, the step S2 shown in Fig. 24 will be described in detail with reference to Fig. 26.

First, in the step S21, the constant component circuit 14 feeds a constant component current Irefc when a load current ID flows.

At the step S22, the CMP1 detects generation of an over-current by the fact that VSA is lower than VSB. On the other hand, it is assumed that an over-current is not generated. Then, processing reverts to the step S21.

When the over-current is generated, the transient component circuit 13 feeds the transient component current Ireft in the step S23.

Moreover, following the step S23, in the step S24, the transient component current Ireft is first fed for a first predetermined time at a constant current value. Next, in the step S25, the transient component current Ireft is decreased within the range such that VSB does not exceed VSA, within the second predetermined time after elapse of the first predetermined time, and is set to almost zero.

(First Semiconductor Switching Device 1)

More specifically, a semiconductor switching device 1 with a first current vibration type shutdown function is composed of circuits as shown in Fig. 2.

A dummy voltage setting circuit 2 can be composed of resistors R1, R2, and R4 and diodes D1 and D2. A numeral assigned to the resistor R1 or the like represents a resistance value in units of Ω. Similarly, a numeral assigned to a capacitor C1 represents a capacity value in units of F.

Two timers for measuring 20 milliseconds and 200 milliseconds start at the same time when a start signal is inputted to an input terminal 1 in the timer 3. A level H is output until 20 milliseconds have been measured from the start in the output terminal 2. A level H is output until 200 milliseconds have been measured from the start in the output terminal 3. This is because an output of a 200 ms timer is inverted by means of an inverter INV1, and is inputted to an input terminal of AND3.

The counter is cleared when a signal is inputted to a reset terminal in the counter 4. The counter counts the number of H to L signals to be inputted to an input terminal connected to the CMP1, and outputs the level H from a 8-pulse output terminal when the number of times is 8. In addition, when the number of times is 32, the level H is outputted from a 32-pulse output terminal.

A shutdown signal holding circuit 5 has a D flip-flop 12. A terminal D is connected to the level H. When an OR circuit inputs a level H to a terminal T, even when the level H disappears, the level H is continuously outputted from an output terminal until a reset signal has been inputted to a reset terminal.

A reference current (Iref) setting circuit 11 can be composed of transistors Tr1 to Tr4, resistors R7 to R10, and a capacitor C1.

A switch SW1 is provided in the externally of a semiconductor chip. A switch SW2 may be further provided. This switching device 1 with the

first current vibration type shutdown function is operated by a user and the like turning ON the switch SW1. In the case where the switch SW2 is provided, this device is operated by turning ON the switches SW1 an SW2. An output voltage VB of a power source VB is set to 12.5V, for example, and an output voltage VP of a charge pump 7 is set to VB + 10V, for example. R6, which is so called a constant component Rrc of a reference resistance Rr, is connected to the QB source electrode. The resistance value of the reference resistor Rrc may be selected according to a ratio "n" of channel widths "W" between QB and QA. For example, as described above, in the case where the ratio "n" of channel widths W between QB and QA is defined as 1:1,000, a value less than a value obtained by multiplying a load resistance value by the ratio "n" (1,000) may be set. Further, in order to finely adjust the resistance value of a reference resistance Rrc, there is utilized the fact that, in the case where the source potential VSA of a main FET (QA) is equal to the source potential VSB of a reference FET (QB), a value obtained by dividing the current (ID) flowing the main FET (QA) by the current (Iref) flowing the reference FET (QB) is defined as a ratio "n". In this case, an attempt is made to feed a current greater than the value obtained by dividing by "n" the current value in the constant state of the load (10). Thus, the resistance value of the reference resistor Rrc is decreased such that VSB is smaller than VSA. By setting this reference resistor Rrc, a drain-source voltage V_{DS} identical to when an over-current exceeding a load current during normal operation flows QA cn be set to a drain - source voltage V_{DS} of QB.

The first semiconductor switching device 1 comprises: Tr5 of a multi-source FET including a main electric field effect transistor (FET: QA) and a reference FET (QB); a voltage comparator CMP1 for comparing a relationship in scale between a QA source potential VSA and a QB source potential VSB; and a driver 8 being a gate driving circuit for, when the QA source potential VSA is greater than the QB source potential VSB, applying a drive voltage to a gate of Tr5, and when the QA source potential VSA is smaller than the QB source potential VSB, shutting down a drive voltage respect to the gate of Tr5. When the current IF at the load 10 side is within a normal range including the transient component, a reference current (Iref) setting circuit 11 for controlling QB current Iref such that the QB source potential VSB does not exceed the QA source potential VSA is disposed between the QB source and grounding.

In this reference current (Iref) setting circuit 11, in the case where the QA source potential VSA is equal to the QB source potential VSB, when a value obtained by dividing the current ID by the current Iref is defined as "n", a constant component (Irefc) circuit flowing a current greater than the value obtained by dividing by "n" the value of the current ID in the constant state of the load 10 and a transient component (Ireft) circuit flowing a current greater than the value obtained by dividing by "n" the value of the current ID in the transient state of the load 10 are disposed in parallel between the QB source and grounding.

Next, an operation of a semiconductor switching device 1 with a first current vibration type shutdown function according to the present invention will be described. When VSA = VSB, a relationship is established as ID (QA drain current) = n x Iref, RL x n = Rr, where VSA denotes a QA source potential; VSB denotes a QB source potential; ID denotes a QA drain current; "n" denotes a current sensing ratio; Iref denotes a QB drain current; RL denotes a resistance (value) of a load connected between QA and GND; Rr denotes a resistance (value) of a reference connected between QB and GND.

Therefore, if VSA > VSB, a relationship is established as ID < n x Iref and RL x n > Rr. If VSA < VSB, a relationship is established as ID > n x Iref and RL x n < Rr. Thus, If Iref or Rr is set as a reference value, it can be judged whether or not a load current value or a load resistance value is greater or smaller than a reference value based on a relationship in scale between VSA and VSB.

When Iref or Rr is set to a value that corresponds to an over-current or an overload, if VSB < VSA, it can be judged as a normal state, and if VSB > VSA, it can be judged as an over-current or overload state. When it is judged as the over-current or overload state, QA and QB are turned OFF. That is, a charge pump voltage Vp applied to the QA and QB gates is shut down via a gate serial resistance, and the QA and QB gates are grounded via a gate serial resistance.

A load current ID or load resistance RL is not generally obtained as a constant value. These values including a component transiently generated like a rush current immediately after a switch has been turned ON and a constant component in the subsequent stable state. The reference current Iref or reference resistance Rr as well are set to a value obtained by combining a transient component and a constant component according to the

load side. That is, Iref or Rr is not constant, and the values are changed with an elapse of time (transiently). This makes it possible to achieve the following: (a) ID < n x Iref or RL x n > Rr can be set respect to the value of ID or RL generated when the load side is normal; and (b) a difference between ID and n x Iref can always be reduced to the minimum.

A constant component (Irefc, Rrc) of Iref or Rr is made available by disposing the resistor R6. If the constant component Irefc of the load current can be regarded as being independent of a voltage in power voltage fluctuation width, the constant component (Irefc) circuit 14 is composed of a constant current circuit instead of the resistor R6.

On the other hand, the transient component (Ireft, Rrt) is made available by a transient component circuit 13 using Tr1 to Tr4, R7 to R10, and capacitor C1 shown in Fig. 2. There are two ways in timing that actually flows a transient component Ireft as follows: (c) a timing when the transient component Ireft is fed in synchronism with an input signal (ON) caused by the switch SW1; and

(d) a timing when the transient component Ireft is fed due to a load fluctuation irrespective of the switch SW1.

A description of (c) can be understood easily. That is, a transient component circuit 13 is started by means of an ON signal of the switch SW1. Specifically, an output terminal of a circuit 6 is connected to a gate electrode of Tr2 of the circuit 13.

Next, a description of (d) will be given. In (d), SW2 is required at the downstream (load side) of QA. Assume that SW1 is turned ON, and SW2 is turned OFF. In this state, although QA and QB are turned ON, SW2 is turned OFF. Thus, a load current does not flow. On the other hand, Irefc always flows via R6. Thus, a relationship is established as Iref x n > ID (= 0), and a relationship is established as VSA > VSB. Then, an output of CMP1 is set to H. The timer and the counter are designed to operate in an input fall cycle. In this state, therefore, the timer and the counter do not operate at all. The timer starts actuation when an input falls. The timer has one output of which a level H is obtained for 20 milliseconds and two outputs of which a level H is established for 200 milliseconds. The timer is designed so as not to accept an input for 200 milliseconds by means of an 200 ms output, INV1, and AND3 once it is actuated. When the timer output 20 ms is set to L, Tr2 and Tr3 (PMOS) is turned OFF. Then, a charge of the capacitor C1 is discharged

based on a base current of Tr4, and a gate potential of Tr1 is set to zero potential. Then, Tr1 is turned OFF, and Iref is obtained as a only current Irefc that flows R6. When SW2 is turned ON in this state, a load current flows through a main FETQA. If this load current is greater than Irefc x n, a relationship is established as VSA < VSB, and an output of CMP1 is changed from level H to level L. The timer and counter operate, and the timer output 20 ms is set to level H. When Tr2 is turned ON, and then, Tr3 is turned ON, a current flows via R9, and C1 is charged up to a voltage close to a power voltage VB. Then, a gate voltage of Tr1 is lifted up to a voltage close to the power voltage, and a transient component Ireft of Iref flows R7. Its scale is expressed by equation 1 below:

Ireft = (VB - Vth)/R7 ... Equation 1

where Vth denotes a threshold voltage of Tr1. While the timer output 20 ms is set to H, Tr2 and Tr3 are maintained to be in ON state, and constant Ireft and Irefc expressed by the above equation 1 flow. At this time, when Ireft is set so as to be Iref x n = (Ireft + Irefc) x n > ID (including transient component), a relationship is established as VSB < VSA. When the timer output 20 ms is set to L, Tr2 and Tr3 are turned OFF, and a charge of the capacitor C1 is discharged as a base current of an NPN transistor Tr4. A discharge time constant is expressed by equation 2 below, where a current amplification rate of Tr4 is defined as hfe4 = 200.

Constant when Tr1 gate potential decreases = C1 x R8 x hfe4 = 0.1 x 10^{-6} x 3 x 10^{3} x 200 = 60 ms ... Equation 2

As a gate potential of Tr1 decreases, Ireft decreases. It is required to disable timer reentry while Ireft decreases to almost zero, and therefore, a 200 ms timer is provided in Fig. 2. Although a constant component circuit is composed of a fixed resistor R6, a constant current circuit may be employed without being limited to the fixed resistor.

On the other hand, a transient component Ireft indicates a first predetermined time when the 20 ms timer is maintained to be in an ON state, a predetermined current value expressed by equation 1. Then, this component decreases within the range such that the source potential VSB does not exceeds the source potential VSA, and the 200 ms timer is set so as to be almost zero within the second predetermined time to maintain the ON state.

When Tr5 is turned ON, i.e., when the semiconductor switching device

1 is turned ON, the constant component circuit is always actuated, and the constant component Irefc flows continuously.

When VSA is lower than VSB, the transient component circuit is started, and the transient component Ireft is fed. Within the required second time such that the 200 ms time is maintained to be in an ON state, even when VSA is lower than VSB, the transient component circuit is not restarted.

Next, an operation of the device 1 containing a dummy voltage setting circuit 2 will be described. The dummy voltage setting circuit 2 includes resistors R1 to R4 and diodes D1 and D2. When QA is fully turned ON, VSA rises up to the power voltage VB, and the driver output of the gate driving circuit 8 rises up to Vp. D1 and D2 are reversely biased, and the dummy voltage setting circuit 2 is isolated from the peripheral circuit, and does not have any effect. However, once the CMP 1 has been set to L, when the gate driver 8 is turned OFF by AND2, R4 is grounded on GND via a sink transistor of the driver 8. Thus, a current flows through paths of power voltage VB → R1 → point B → D1 → point A → D2 → R4 → driver sink transistor → GND, and a potential at point A is lowered. At this time, the potential at point A is calculated under the condition such that no current through R3 is inputted and outputted. A circuit from R1 to R2 can be expressed by equation 3, and a circuit from R1 to R4 through points B and A can be expressed by equation 4.

10K (I1 + I2) + 24K x 12 = 12.5 (V) ... Equation 3

10K (I1 + I2) + 3.3K x 11 + 0.6 x 2 = 12.5 (V) ... Equation 4

From equations 3 and 4, I1 = 0.736A and I2 = 0.151A are obtained. Therefore, the potential at point A is obtained as in equation 5. On the other hand, when I1 = 0, a potential at point B is obtained as in equation 6.

(Potential at point A) = 3.03V ... Equation 5

(Potential at point B: I1 = 0) = 8.82V ... Equation 6

In the circuit shown in Fig. 1, the potential at point A differs from the value shown in equation 5 because a current is inputted or outputted through resistor R3. When the current flowing resistor R3 is set to zero, i.e., when potential at point A = VSA, 3.03V is obtained. When the potential at point A is smaller than VSA, it is obtained according to equation 7 below.

Potential at point A = VSA - (R3 voltage fall) ... Equation 7

That is, once QA has been turned OFF, a potential lower than VSA is

inputted to a + input terminal of CMP1. Therefore, even when VSA vibrates to some extent, if the vibration width is smaller than an R3 voltage fall, CMP1 is stabilized to maintain L. When QA is continuously turned OFF, VSA is lowered toward GND, and the QA gate potential is lowered. The GB gate is directly linked with the QA gate, and thus, VSB is lowered as VSA is lowered. As VSA is lowered, although the potential at point A is slightly lowered, its lowering quantity is slight.

On the other hand, VSB is continuously lowered together with the lowering of VSA. The potential at point A is supplied to the "+" terminal voltage of CMP1, and a potential of VSB is supplied to the "-" terminal. Thus, a relationship is established as "+" terminal potential of CMP1 > "-" terminal potential of CMP1, and an output of CMP1 is inverted from L to H. This inversion occurs irrespective of the state on the load side, i.e., even when VSA < VSB. In this manner, the gate driver is turned ON again, QA and QB are turned ON, and VSA and VSB turn to rise. Since the gate driver output rises from 0V to Vp, D2 is reversely biased, and the potential at point A rises as VSA rises. At this time, a relationship is established as potential at point A > VSA. This state continues until the potential at point A is equal to that at point B (potential obtained by pressure dividing the power voltage VB by R1 and R2). At this time, the potential at point B is equal to a voltage obtained by pressure dividing the power voltage VB by R1 and R2, and 8.82V is obtained from equation 6.

In short, the dummy voltage setting circuit 2 serves to forcibly turn ON QA and QB when VSA is obtained as a dummy voltage L (potential at point A) expressed by equation 5 or less, and maintain QA and QB to be ON irrespective of the state of the load side until VSA has been set to a dummy voltage H (potential at point B) or more expressed by equation 6. When VSB exceeds a value of equation 6, it is determined whether QA and QB are turned ON/OFF according to a relationship in scale between VSA and VSB.

When a timing of starting setting of a transient component (Ireft or Rft) is executed according to the method of (d), this switching device 1 can be used instead of a fuse. In the case where the device is used instead of the fuse, SW1 is set to an ON. A load is controlled to be turned ON/OFF by SW2. That ON/OFF signal is not inputted to this switching device 1. Although it is required to start setting of a transient component (Ireft) when a load current (ID) changes, the system of (d) meets this requirement. In addition,

even when this device is used as a general switching device so as to be turned ON/OFF by SW1, the setting of the transient component (Ireft) can be started without any problem.

On the other hand, when the timer output 20 ms is set to H, Ireft is set, and a relationship is established as VSA > VSB, the QA and QB that have been temporarily turned OFF are turned ON again by a dummy voltage L (potential at point A). Then, as long as a load circuit is normal, in other words, as long as a wiring short-circuit or the like does not occur, QA and QB are continued to be ON.

In the dummy voltage setting circuit 2, after VSA is lower than VSB, when QA and QB are switched OFF, such VSA is compared with VSB by using the potential at point A that falls into a lower dummy voltage level L instead of VSA. If VSB is lower than a dummy voltage level L, QA and QB are switched ON.

Until a potential at potential B has been obtained in equation 6 in which VSB rises, and a dummy voltage level H greater than the dummy voltage level L is obtained, QA and QB are maintained to be turned ON irrespective of a relationship in scale between VSA and VSB. When VSA exceeds the dummy voltage level H (potential at point B), VSA is compared with VSB. If VSA is smaller, QA and QB is switched OFF.

Therefore, as long as VSA is lower than VSB, ON/OFF operation is continued.

After QA and QB repeat ON/OFF operation by predetermined times, the multi-source FET (Tr5) is shut down. This shutdown is performed in two cases, i.e., in the case where eight ON/OFF operations are performed within a first predetermined time of the 20 ms timer and in the case where 32 ON/OFF operations are performed in a second predetermined time of the 200 ms timer.

While a 20 ms output of the timer 3 is set to H, in the case where an over-current state Iref x n < ID or an overload state Rr > RL x n is established, when the voltage comparator CMP1 repeats eight outputs of high/low (H/L), QA and QB are shut down. In the former case, a dead shorting state is established. In this case, the heating of QA due to ON/OFF operation is great, and thus, QA and QB are shut down for a minimally short time. In the latter case, the over-current value is smaller than that in the former case, the heating of QA is reduced. Thus, 32 ON /OFF operations are performed by taking high priority over thorough check. However, it is more preferable

that 32 ON/OFF operations be reduced to eight ON/OFF operations, and such eight ON/OFF operations can be performed in any case.

(First Embodiment (According to First Semiconductor Switching Device 1))

In the first embodiment, an operation of the first switching device 1 when a normal lamp load is used will be described here. A case in which a lamp does not function as a shutdown function, lights, and continuously lights is assumed. A lamp load 10 is employed as a load having two 21W bulbs connected in parallel. Fig. 3 is a graph showing a signal waveforms of a switching circuit 1 when the bulb lights. A time of 50 milliseconds per scale is taken on a horizontal axis. On a vertical axis, there are taken a source potential (VSA) of the main FET (QA) of Tr5; a voltage representing a timer output of 200 milliseconds outputted at an output terminal 3 until 200 milliseconds have been measured from the start of the timer 3; QA drain current ID; and drain current Iref of the reference FET (QB) of Tr5 obtained by "n" times. A unit of the vertical axis are shown at the right side of a respective one of VSA, ID, and Iref in the graph. The VSA vertical axis is represented as (2V/div, 6V), one scale denotes 2V, and a voltage of the fourth scale of all the eight scales is defined as 6V. Similarly, the vertical axis of ID and n x Iref is represented as (10A/div, 30V), and one scale is defined as 10A, and the current of the fourth scale of all the eight scales is defined as 30A. In the following graph as well, the vertical axis is represented by a similar measurement system.

A timer output is turned ON at the first scale of the time axis, and is turned OFF 180 milliseconds after the timer output has been turned ON. ID starts flowing at the same time when the timer output has been turned ON. Although the starting current value reaches 30A, the value then decreases, and becomes constant at 4A before the timer output is turned OFF. ID is a current that flows a lamp load, and the lamp lights when the current starts flowing. When the current value is obtained as 4A, the lamp normally lights continuously. This current 4A is obtained as an ID constant component, and a component is obtained as a transient component by subtracting a component of the current 4A from the current value that exceeds the current 4A when the current starts flowing. As n x Iref, 5A of the constant component "n x Irefc" starts flowing at the same time when the timer output has been turned ON. Although this starting current value reaches 40A, the value then decreases, and the transient component n x Ireft is eliminated

before the timer output is turned OFF. Then, only 5A of the constant component n x Irec becomes constant. The ID current value is smaller than n x Iref at any time as well. Therefore, it can be judged VSA is greater than VSB at any time as well, and a over-current is not generated. In VSA, a voltage increases at the same time when the timer output is turned ON, and a voltage exceeding 12V is applied to the lamp load 10. When n x Iref > ID, FET is continued to be turned ON.

The waveforms of VSA, ID, and n x Iref in Fig. 4 are identical to those shown in Fig. 3. The figure shows a relation with a 20 ms timer 3, and the time axis on the horizontal axis is enlarged to 5 times. From the foregoing, it is found that n x Iref is fixed to about 40A from a signal of the 20 ms timer 3 is turned from ON to OFF, and the value decreases after the signal has been turned OFF.

The waveforms of VSA, ID, and n x Iref in Fig. 5 are identical to those shown in Figs. 3 and 4. The figure shows a relation with an ON signal of an input signal (gate driving signal) of a driver 8 caused by switch SW1 or the like generated when SW1 is turned ON, wherein the time axis of the vertical axis shown in Fig. 4 is further enlarged to 10 times. Therefore, due to a rise delay of a charge pump 7, a delay of about 80 microseconds is produced from ON of the SW1 input signal (gate driving signal) to a fall of ID or the like.

The waveforms of VSA, ID, n x Iref, and gate driving signal in Fig. 6 are identical to those shown in Fig. 5. The rise time of the waveforms of VSA, ID, and n x Iref shown in Fig. 5 is enlarged to 10 times shown in Fig. 5. In this manner, ID is greater than n x Iref after the time of three scales and a half. By this reversal, the gate driving signal is turned OFF, and the increasing VSA turns to decrease. Then, when VSA decreases, and a dummy voltage level is equal to or less than L (potential at point A), an input signal is turned ON again, and VSA, ID, and n x Iref rises.

(Second Embodiment (According to First Semiconductor Switching Device 1))

In a second embodiment, a description will be given with respect to an operation of a first switching device 1 in the case where a lamp load is further added, and an overload state occurs when a normal lamp load lights. When the lamp lights, if an attempt is made to illuminate another lamp, the shutdown function works, and all the lamps are turned OFF. A lamp load having two 21W bulb lamps connected in parallel is used as a lamp load that initially lights. One 21W bulb lamp is used as an additional lamp load for

overload, and is connected in parallel to two lighting lamps. Fig. 7 is a graph showing signal waveforms of a switching circuit until an overload has been added and shut down when a bulb lights. A time of 20 milliseconds per scale is taken on the horizontal axis. VSA, input signal (gate driving signal) to driver 8, ID, and n x Iref are taken on the vertical axis. When n x Iref falls, n x Iref < ID is established, and QA is shut down.

The waveforms of VSA, ID, n x Iref, and input signal (gate driving signal) shown in Fig. 8 are identical to those shown in Fig. 7. A rise time of the waveforms of VSA, ID, and n x Iref shown in Fig. 7 is enlarged to 2,000 times shown in Fig. 7. The respective waveforms are changed in the same way as in Fig. 6. ID is greater than n x Iref after the time of four scales and a half. By this reversal, the gate driving signal is turned OFF, and VSA starts decreasing. Then, when VSA decreases, and a dummy voltage is equal to or less than level L (potential at point A), the gate driving signal is turned ON again, and VSA, ID, and n x Iref rises as well. Therefore, three lamps including such additional one lamp are turned OFF.

The waveforms of VSA, ID, n x Iref, and input signal (gate driving signal) shown in Fig. 9 are identical to these shown in Fig. 7. A time to be shut down at a fall of VSA, ID, and n x Iref waveforms shown in Fig. 7 is enlarged to 400 times shown in Fig. 7. ID is slightly greater than n x Iref in front of a time scale of 1/4. By this reversal, an input signal (gate driving signal) is turned OFF again, and VSA and VSB (not shown) decreases. The pulse counter 4 counts this decrease count. When VSB decreases, and a dummy voltage is equal to or less than level L (potential at point A), an input signal (gate driving signal) is turned OFF again, and VSA, ID, and n x Iref increases as well. When VSB increases, and a dummy voltage is equal to or less than level H (potential at point B), an input signal (gate driving signal) is turned OFF again, and VSA, ID, and n x Iref decreases as well. In this way, when the waveforms are fluctuated, and VSA and VSB decreases to the 32 times, the input signal (gate driving signal) is fixed to be OFF, and VSA, ID, and VSB (not shown) are not outputted. Therefore, three lamps including such additional one lamp are turned OFF. A time required from generation of over-current to current shutdown is set to 450 microseconds.

The waveforms of VSA and input signal (gate driving signal) shown in Fig. 10 are identical to those shown in Fig. 9. A time shut down at a fall of the waveforms of VSA and input signal (gate driving signal) shown in Fig. 9 is

enlarged to five times shown in Fig. 9. A voltage at point A is defined as a dummy voltage. It is found that the voltage at point A has a level H (so called point at point B) of 7V to 8V and level L of about 3V to 4V (so called potential at point A). VSB (not shown) is fluctuated from level L to level H and from level H to level L similar to VSA.

(Third Embodiment (According to First Semiconductor Switching Device 1)

In a third embodiment, a description will be given with respect to a first switching device 1 when a lamp load being overload is used. A lamp does not light because a shutdown function works. A lamp load 10 is employed as a load having three 21W bulb lamps connected in parallel. In the device 1, n x Iref is set such that overload is obtained by three lamps rather than two lamps. Fig. 11 is a graph showing signal waveforms of a switching circuit from driver input signal ON to shut down. A time of 100 microseconds per scale is taken on the horizontal axis. VSA, input signal, ID, and n x Iref are taken on the vertical axis. QA is shut down when eight ON/OFF operations are repeated. In a process in which ID and n x Iref is increased each time, ID that has been smaller than n x Iref is greater than n x Iref close to 135A. By this reversal, QA and QB are turned OFF. VSA and VSB (not shown) turns from increasing to decreasing. When VSB decreases, and a dummy voltage is equal to or less than level L, an input signal is turned ON. VSA and VSB increase again. In this way, VSA and VSB are fluctuated.

(Second Semiconductor Switching Device 1)

A semiconductor switching device 1 with a current vibration type shutdown function can be composed of a circuit as shown in Fig. 12.

A dummy voltage setting circuit 2, a timer 3 and a D flip-flop 12 serving as a shutdown signal holding circuit 5 is identical to the first semiconductor switching device 1 shown in Fig. 2. A pulse counter 4 employs a four-pulse counter 14, unlike Fig. 2. When a signal is inputted to a reset terminal, the count is cleared. When the count of signals from H to L inputted to an input terminal connected to CMP1 is counted, and four is counted, level H is outputted from an output terminal. A reference current circuit 11 changes from 3 KΩ to 1 KΩ in resistance value of a resistor R8.

A second semiconductor switching device 1 comprises: Tr5 that is a multi-source FET including QA and QB; a voltage comparator CMP1 for comparing a relationship in scale between QA source potential VSA and QB

source potential VSB; and a gate driving circuit 8 for applying a drive voltage to a gate of Tr5 when VSA is greater than VSB, and showdown a drive voltage to a gate of Tr5 when VSA is smaller than VSB.

Further, in the semiconductor switching device 1, in the case where VSA is equal to VSB, assuming that a value obtained by dividing by current ID following QA by current Iref following QB is defined as "n", a constant component (Irefc) circuit that flows a current Irefc greater than a value obtained by dividing by "n", a value of a current ID in a constant state when a load 10 is within a normal range and a transient component (Ireft) circuit in which a current Ireft greater than a value obtained by dividing "n" a current value in a transient state when the load 10 is within a normal range are disposed in parallel between the reference FET (QB) source and the grounding.

When a current flowing the load 10 rapidly increases, and a source potential VSA of a main FET is smaller than a source potential VSB of a reference FET, the device is configured so as to start a transient component Ireft. If a phenomenon that a transient component circuit 13 is restarted within a third predetermined time after the transient component circuit 13 has started is repeated by a predetermined time, a multi-source FET (Tr5) is shut down.

In the case where only a constant component circuit 14, or in the case where the constant component circuit 14 and transient component circuit 13 operate, when VSA is smaller than VSA, CMP1 outputs a reversal pulse, and a timer 3 restarts. The 20 ms timer 3 is maintained to be turned ON again by this restart, and thus, the transient component circuit 13 restarts.

After this restart, if a phenomenon that the transient component circuit 13 is further restarted again within a time such that the 200 ms timer 3 is maintained to be turned ON is repeated by predetermined four times, QA is shut down. That is, the timer 3 is restarted within a time such that the 200 ms timer 3 is maintained to be turned ON. Because of the restart, the 200 ms timer 3 is continuously maintained to be turned ON. Thus, the four-pulse counter 14 is not reset. The inversion pulse of CMP1 is regarded as a continuous pulse by means of the counter 14, and the vibration count of counted as vibration.

Next, a description will be given with respect to an operation of a semiconductor switching device 1 with a second current vibration type

shutdown function according to the present invention. Judgment between VSA and VSB in scale, setting of Iref or the like, and operation of a dummy voltage circuit are identical to those according to the first embodiment. However, a resistor R8 or the like are changed. Thus, if the timer output 20 ms is set to L, Tr2 and Tr3 are turned OFF. A charge of capacitor C1 is obtained as a base current of NPN transistor Tr4, and discharge time constants are different from each other. The discharge time constant is expressed by equation 2 where the current amplification rate "hfe4" of Tr4 is equal to 257.

Constant when Tr1 gate potential decreases = C1 x R8 x hfe4
$= 0.1 \times 10^{-6} \times 1 \times 10^{3} \times 257 = 25.7$ ms ... Equation 8

As Tr1 gate potential decreases, Ireft decreases. After an output of a 200 ms timer 3 has been connected to a reset terminal of a four-pulse counter 14, when an output of the 200 ms timer 3 is set to level H, a four-pulse counter 14 operates. When the timer is set to level L, the four-pulse counter 14 is reset.

On the other hand, when the timer output 200 ms is set to H, Ireft is set, and VSA > VSB, if a load circuit is normal after QA and QB that have been temporarily turned OFF is turned ON again, in other words, if a wiring short-circuit or the like occur, QA and QB are continued to be turned ON.

While an output 20 ms of the timer 3 is set to H, in the case where the over-current state Iref x n < ID or the overload state Rr > RL x n, QA and QB are shut down when CMP1 repeats ON/OFF operation four times. This is a dead short-circuit state. In this case, the heating of QA caused by ON/OFF operation is great, thus making it possible to shut down them for a minimally short time.

In addition, in the case where the timer output 20 ms is set to L, and the over-current or overload state is established, the output of CMP1 changes from H to L. Thus, the timer output 20 ms is set to H, and Iref transient component Ireft restarts. At the same time, the output of the 200 ms timer 3 is set to H. Therefore, if a transient component Ireft restarts within 200 ms after the first transient component Ireft has started, the CMP1 output rise count is integrated without the four-pulse counter 14 being reset. As shown in Figs. 13 (a) and 13 (b), if the transient component Ireft is continuously restarted four times with an interval of within 200 ms regarded as a continuous pulse (vibration), the four-pulse counter 14 overflows, and outputs

an output signal. QA and QB are shut down. The output of the 20 ms timer 3 is under the condition such that the CMP1 output rise count is integrated. So called the continuity of the continuous pulse is defined.

In this way, a method for restart a transient component a maximum of four times before shutting down the multi-source FET Tr5 has the following effects.

(1) When the transient component Iref is too short, and is zero when the normal transient component on the load side still remains, even in the case where Iref x n < ID, the transient component is restarted, whereby incorrect shutting down of FET can be avoided. If the load is normal, the load transient component is set to zero until the transient component Ireft has been restarted four times.

(2) As shown in Fig. 13 (c), even in the case where a plurality of leads are restarted with a short interval of within 200 ms, if the respective loads are normal, a switch can be turned ON without incorrect shutdown. That is, in a four-pulse counter system, up to three loads can be employed to prevent incorrect shutdown. In the case where a load increases, the counter setting is increased, thereby making it possible to prevent incorrect shutdown.

(3) In the case where chattering has occurred when the switch is turned ON, incorrect operation can be avoided as in the same way as in (2).

(4) A time required for shutdown changes depending on a degree of abnormality. That is, during dead short-circuit, shutdown is achieved within 100 microseconds to 150 microseconds in the four-pulse counter. In Fig. 11 in the case of eight pulses, a time about 300 microseconds is required for shutdown. If four pulses are obtained, shutdown can be achieved at about half of the above time, as shown in Figs. 18 to 20 described later. In addition, if an overload is light, four rechecks are performed, and shutdown is achieved within 400 milliseconds to 600 milliseconds with time intervals.

In the case of a dead short-circuit, there is a low possibility of incorrect judgment, and quick shutdown is effective in protection of wires and elements. In addition, in the case where a degree of abnormality is light, there is a high possibility of incorrect judgment, and thus, re-judgment with increased time intervals is effective in avoiding incorrect judgment. In the case where a degree of abnormality is light, the wires and elements are less heated, and thus, there is no problem caused by an increased shutdown time. Therefore, this system is reasonable for protection of over-current or overload.

Moreover, in the case where a degree of abnormality is light, as shown in Figs. 13 (a) and 13 (b), as the scale of the current ID increases, a time from turning ON the load 10 to FET shutdown can be reduced.

(5) It is possible to detect intermittent overload and over-current. In the timer output 200 ms, only an intermittent abnormality within 200 ms can be detected. However, a long intermittent abnormality can be detected by increasing 200 ms. However, increasing the timer output causes more frequent malfunctions, and thus, such increase of the timer output in random is not preferable.

(Fourth Embodiment (According to Second Switching Device 1))

In a fourth embodiment, an description will be given with respect to an operation of a second switching device 1 when a normal lamp load is used. As in the first embodiment, a case in which a lamp does not function as a shutdown function, lights, and continuously lights is assumed. A lamp load 10 is employed as a load having two 21W bulbs connected in parallel.

Fig. 14 is a graph showing a signal waveform chart of a semiconductor switching device 1 when a bulb lights. The horizontal axis represents time, one scale is defined as 10 milliseconds. On the vertical axis, there are taken: a voltage representing a source potential (VSA) of Tr5 main FET (QA) and a 20 millisecond timer output outputted at an output terminal 2 until 20 milliseconds have been counted from the start of a timer 3; a QA drain current ID; and a drain current n x Iref of Tr reference FET (QB). A unit of the vertical axis is indicated on the right of a respective one of VSA, ID, and Iref in a graph. The vertical axis of VSA is represented as (2V/div, 6V), one scale is defined as 2V, and a voltage of the fourth scale of all the eight scales is defined as 6V. Similarly, the vertical axis of ID and n x Iref is represented as (10A/div, 30V), one scale is defined as 10A, and a current of the fourth scale in all the eight scales is defined as 20A. In the following graph as well, the vertical axis is expressed by a similar measuring system.

An output of the 20 ms timer 3 is turned ON at a first scale of the time axis, and is turned OFF 18 milliseconds after the timer has been turned ON. ID starts flowing at the same time when the timer output is turned ON. Although the starting current value reaches 30A, the value then decreases, and is lowered to 8A when the timer output is turned OFF. ID is a current that flows the lamp load 10, and the lamp 10 lights when the current starts flowing. When the current value is further lowered to 4A, the lamp 10

continuously lights normally. This current 4A is a constant component of ID, and a component obtained as a transient component by subtracting a component of current 4A from a current value that exceeds current 4A when the current starts flowing. For n x Iref, 5A of a constant component n x Irefc flows before the time output is turned ON. This starting current value reaches 40A. n x Iref from a time when signal of the 20 ms timer 3 is turned ON to that when the timer is turned OFF is fixed to about 40A, and decreases after the timer has been turned OFF. The ID current value is lower than n x Iref at any time. Therefore, VSA is greater than VSB at any time, and an over-current is not generated. For VSA, a voltage is increased at the same time when the timer output is turned ON. A voltage exceeding 12V is applied to a lamp load 10. When n x Iref > ID, FET is continued to be turned ON.

The waveforms of VSA, ID, and n x Iref shown in Fig. 15 are identical to those shown in Fig. 14. The figure shows a relation with an ON signal of an input signal (gate driving signal) of a driver 8 such as SW1 generated when the switch SW1 is turned ON. Depending on a rise delay of a charge pump 7, a delay of about 80 milliseconds occurs from when SW1 input signal (gate driving signal) is turned ON to a rise of ID or the like.

The waveforms of VSA, ID, and n x Iref shown in Fig. 16 are identical to those shown in Fig. 15. A rise time of the waveforms of VSA, ID, and n x Iref shown in Fig. 15 is enlarged to 10 times shown in Fig. 15. Therefore, ID is greater than n x Iref at a time of three scales and a half. By this reversal, a gate driving signal is turned OFF, and the increased VSA and VSB (not shown) turn to decrease. Then, when VSB decreases, and a dummy voltage is equal to or less than level L (potential at point A), an input signal (gate driving signal) is turned ON again, and VSA, VSB, ID, and n x Iref rise as well.

The waveforms of VSA, ID, and n x Iref in Fig. 17 are identical to those in Fig. 14. The figure shows a relation with a 200 ms timer 3, where the time axis on the horizontal axis is reduced to 1/5. Therefore, the timer output 200 ms is turned ON at the first scale of the time axis, and is turned OFF 180 milliseconds after the output has been turned ON. ID starts flowing at the same time when the timer output is turned ON. Although the starting current value reaches 30A, the value then decreases, and is constant at 4A before the timer output is turned OFF. For n x Iref, 5A of a constant

component n x Irefc flows before the timer output is turned ON. Then, a transient component n x Ireft starts flowing at the same time when the timer output is turned ON. Although this starting current value reaches 40A, the value then decreases. A transient component n x Ireft is eliminated before the timer output is turned OFF, and only 5A of the constant component n x Irefc becomes constant.

(Fifth Embodiment 5 (According to Second Semiconductor Switching Device 1))

In a fifth embodiment, a description will be given with respect to an operation of a second semiconductor switching device 1 according to the present invention when wiring between QA and a load 10 is dead-shorted.

Fig. 18 shows the waveforms when switch SW1 is turned ON while wiring between QA and the load 10 is dead-shorted.

ID flowing in shorted state exceeds Iref, and thus, QA and QB that have been temporarily turned ON are turned OFF. A voltage lower than VSA is inputted to a + input terminal of CMP1. Thus, even when VSA slightly fluctuates, if its fluctuation width is smaller than a voltage fall of R3, CMP1 is stabilized, and a dummy voltage is maintained to level L (potential at point A in equation 5 and point A in Fig. 18). When QA continues to be turned OFF, VSA is lowered toward GND, and QA gate potential is lowered as well. QB gate is directly linked with QA gate, and thus, as VSA is lowered, VSB is lowered. As VSA is lowered, the potential at point A is slightly lowered, but its lowering quantity is slight. The potential at point A is supplied to a + terminal voltage of CMP1, and the potential of VSB is supplied to a - terminal, thus, a relationship is established as + terminal potential of CMP1 > - terminal potential of CMP1, and an output of CMP1 is reversed from L to H. A gate driver 8 is turned ON again, QA and QB are turned ON, and VSA and VSB turn to rise. An output of the gate driver 8 rises from 0V to Vp, and thus, D2 is reversely biased. The potential at point A rises as VSA rises. At this time, a relationship is established as potential at point A > VSA. The potential at point A rises up to the potential at point B in equation 6 (dummy voltage level H and point B in Fig. 18). After VSB has risen by turning QB, when a dummy voltage is equal to or more than H, an output of CMP1 is inverted from H to L. The pulse counter 14 counts a first count. The gate driver 8 is turned OFF again, and QA and QB are turned OFF. QA and QB are repeated to be turned ON/OFF, and the counter

14 increases the number of counts every time. A signal from the counter 14 is outputted at a fourth count, the gate driver 8 is turned OFF again, and QA and QB are turned OFF. A time required from generation of short-circuit to current shutdown is set to 110 microseconds.

Fig. 19 is the waveforms when a load 10 are employed as a load having two 21W bulb lamps connected in parallel, thereby dead-shorting wiring between QA and the load 10 when two lamps light. ON/OFF operations of QA and QB similar to those shown in Fig. 18 are repeated. A time required from generation of short-circuit to current shutdown is set to 130 microseconds.

(Sixth Embodiment (According to Second Semiconductor Switching Device 1))

In a sixth embodiment, an operation will be described with respect to a second switching device 1 when a lamp load being an overload is used. A lamp does not light because a shutdown function works. A lamp 10 is employed as a lamp having three 21W bulb lamps connected in parallel. In the device 1, n x Iref is set such that an overload is obtained by three lamps without such overload being obtained by two lamps. Fig. 20 is a graph showing signal waveforms of a switching device from driver input signal ON to shut down. A time of 20 microseconds per scale is taken on the horizontal axis. VSA, gate driving signal, ID, and n x Iref are taken on the vertical axis. A multi-source FET Tr5 is shut down at a time when ON/OFF operations are repeated four times. In a process in which ID and n x Iref are greater each time, ID that has been smaller than n x Iref is greater than n x Iref close to 35A. By this reversal, a gate driving signal is turned OFF, and VSA turns from increase to decrease. When VSA decreases, and is equal to or less than level L of a dummy voltage, an input signal is turned ON, and VSA increases again. In this way, VSA vibrates. The four-pulse counter 14 counts vibration of VSA via CMP1. When this count falls into a fourth count, the counter 14 outputs an ON signal, and an input signal of the driver 8 is turned OFF. When this fourth count is obtained, the timer 3 is also turned ON, and Iref flows. Therefore, ID is recovered to be smaller than n x Iref. This recovery does not cause VSA and ID to be turned ON again. Three lamps of the load 10 are turned OFF. A time required from switch ON to current shutdown is set to 185 microseconds.

(Seventh Embodiment (According to Second Semiconductor Switching Device 1))

In a seventh embodiment, a description will be described with respect to an operation of a second switching device 1 in the case where an overload state occurs when a normal lamp load lights, and further, a lamp load is added. When a lamp lights, if an attempt is made to further illuminate another lamp, a shutdown function works, and all the lamps are turned OFF. A lighting lamp load from the start is employed as a lamp having two 21W bulb lamps connected in parallel. A lamp load to be added for overload is used as a load having one bulb lamp connected to the lighting two lamps. Fig. 21 is a graph showing signal waveforms of a switching circuit until shutdown has been achieved after an overload has been added during bulb illumination. A time of 50 milliseconds per scale is taken on the horizontal axis. VSA, input signal to driver 8, ID, and n x Iref are taken on the vertical axis.

The waveforms shown in Fig. 21 correspond to those in the case of a middle overload shown in Fig. 13 (a) and a small overload shown in Fig. 13 (b). Ireft of n x Iref starts four times repeatedly. A start interval is set to about 105 milliseconds, and is smaller than 200 ms of the timer 3. A time required from generation of an over-current to current shutdown is set to 420 milliseconds.

The waveforms of VSA, ID, n x Iref, and input signal in Fig. 22 are identical to those in Fig. 21. A rise time of the waveforms of VSA, ID, and n x Iref in Fig. 21 is enlarged to 5,000 times in Fig. 21. The respective waveforms are changed in the same way as in Fig. 8. ID is greater than n x Iref at a time of four scales and a half. By this reversal, the gate driving signal is turned OFF, and VSA starts decreasing. Then, if VSA decreases, and is equal to or less than level L of a dummy voltage, the gate driving signal is turned ON again, and VSA, ID, and n x Iref increase as well. Three lamps including thus added one lamp are turned OFF.

The waveforms of VSA, ID, n x Iref, and input signal in Fig. 23 are identical to those in Fig. 21. A time at which a rise of the waveforms of VSA, ID, and n x Iref shown in Fig. 21 is shut down is enlarged to 5,000 times shown in Fig. 21. ID is slightly greater than n x Iref, whereby an input signal is turned OFF, and VSA decreases. The four-pulse counter 14 counts this decrease. This count falls into a fourth count, and thus, the counter 14 outputs an ON signal. An input signal of the driver 8 is turned OFF. When this fourth count is obtained, the timer 3 is turned ON, and Iref flows.

Therefore, ID is recovered to be smaller than n x Iref. This recovery does not cause VSA and ID to be turned ON again. Three lamps including added one lamp are turned OFF.

As described above, according to the present invention, there can be provided a semiconductor switching device capable of detecting an over-current even when a rush current is generated, and capable of responding at a high speed to an over-current in the case where a rare short-circuit such as incomplete shot-circuit having a certain short-circuit resistance is generated.

In addition, according to the present invention, a reference circuit includes a constant component and a transient component. Thus, a normal state is handled respect to a transient phenomenon (transient component) generated on the load side, and ON/OFF operation is not performed. Thus, a problem such as lamp illumination delay is eliminated, and the heating of an element can be reduced.

According to the present invention, a transient component of the reference circuit can be started according to a change on the load side, thus, making it possible to substitute a fuse function.

According to the present invention, a dummy voltage of two levels is employed for current vibration control. Thus, a delay element of a gate driving circuit of a multi-source FET is not required, ON/OFF operation is stabilized, and ON/OFF operation characteristics can be easily controlled.

According to the present invention, a transient component is incorporated in a reference, thus making it possible to change a shutdown time when an abnormality occurs due to a scale of the transient component. Specifically, in the case where an abnormality occurs when the transient component is great or in the case where such abnormally has occurred, a method for achieving shutdown for a short time can be employed. Thus, even in the case where a current restriction during dead-shorting is insufficient, a time required for shutdown is reduced, thereby making it possible to reduce a wire. In addition, the heating of an element can be restricted, making it unnecessary to provide a specific current restriction circuit. In this manner, a control circuit is simplified, thus making it possible to reduce an element chip area or integrate the FET and control circuit on one chip, resulting in cost reduction.

Further, according to the present invention, the ON/OFF control count

of the semiconductor switch due to control means (control steps) is counted by means of a pulse counter. When this control count reaches a predetermined count, the semiconductor switch is controlled to be turned OFF. Thus, even in incomplete short-circuit, the shutdown of the semiconductor switch can be accelerated to an arbitrary set time, and a high speed response can be achieved.

In particular, in the case where ON/OFF control of the semiconductor switch is integrated in a monolithic manner, no microcomputer is required. Thus, a chip area can be reduced, and equipment cost can be remarkably reduced.

Various modifications will become possible for those skilled in the art after receiving the teachings of the present disclosure without departing from the scope thereof.